

PRIOR ART

Fig. 1

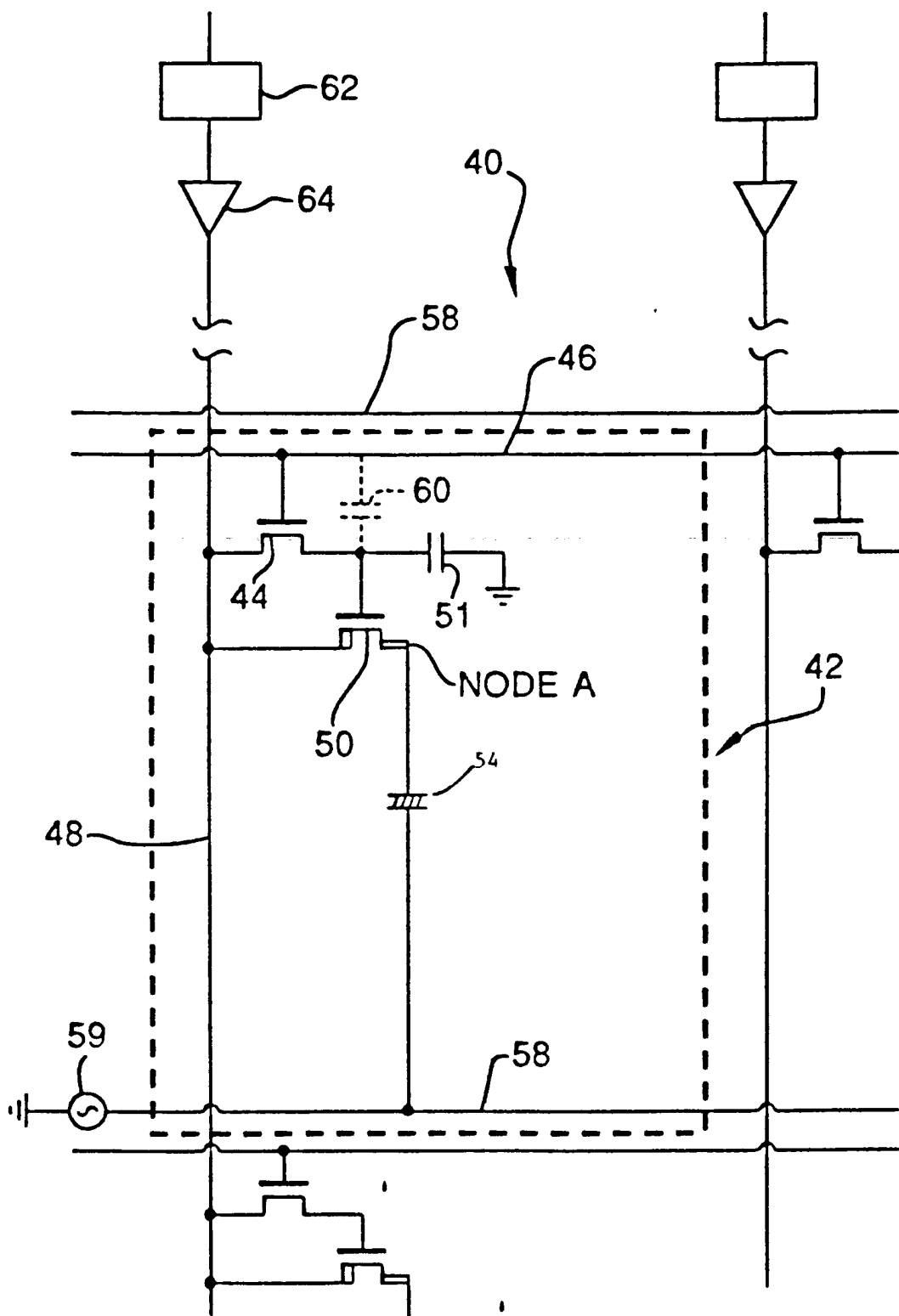


Fig. 2

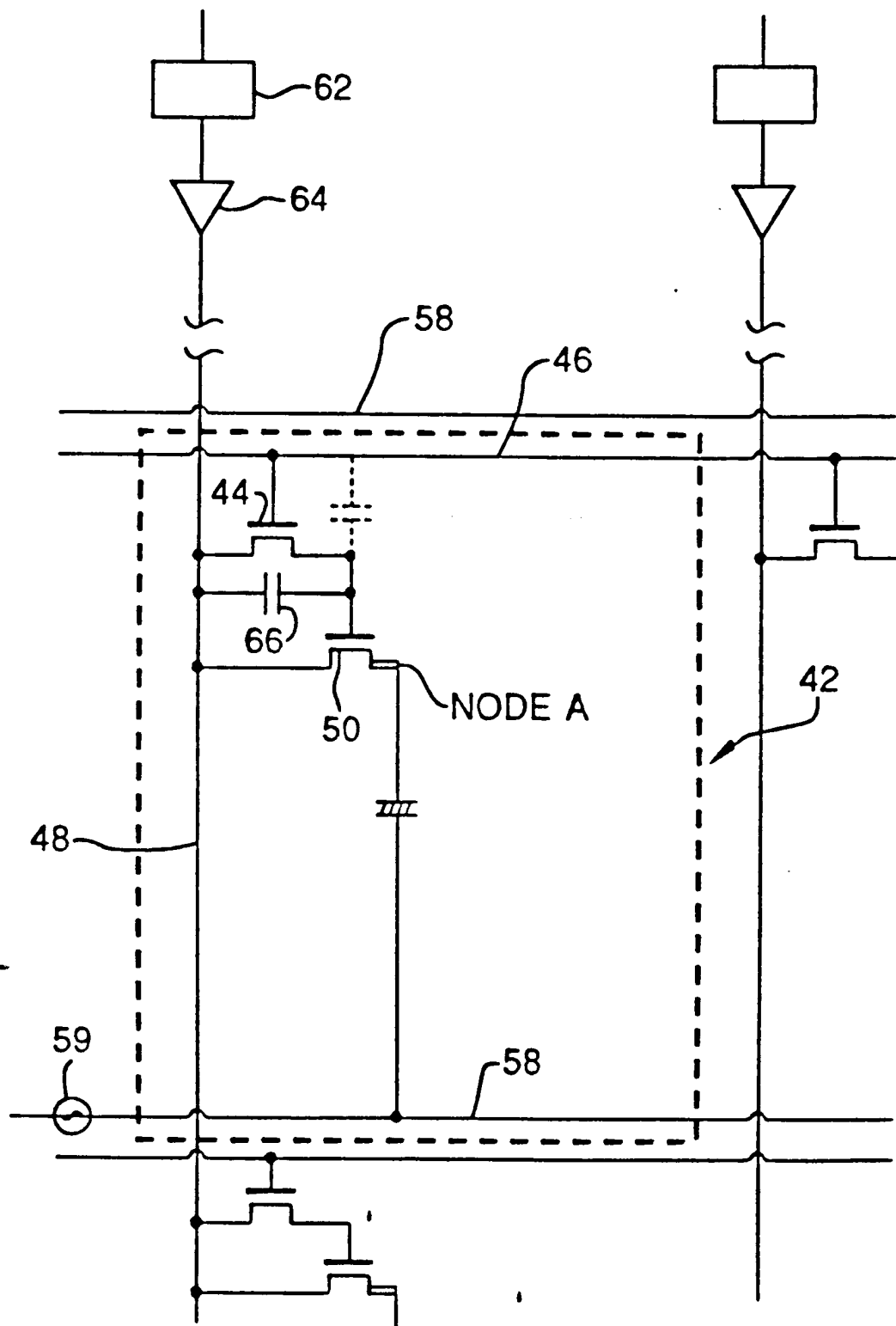


Fig. 2(a)

The diagram shows a differential amplifier circuit. Two input nodes, labeled 60 and 62, are connected to the gates of two NMOS transistors, 64 and 70. The drains of these transistors are connected to a common output node, labeled 66. A current mirror load is connected between the output node 66 and a common ground node, labeled 78. The current mirror consists of two PMOS transistors, 72 and 74, connected in series. The gate of transistor 72 is connected to its drain, and the gate of transistor 74 is connected to the gate of transistor 72. The source of transistor 74 is connected to the common ground node 78. The source of transistor 72 is connected to the output node 66. The gates of both transistors 72 and 74 are connected to a bias voltage, labeled 76. The output node 66 is also connected to a load resistor, labeled 68, which is connected to a supply voltage, labeled 60. The output node 62 is also connected to a load resistor, labeled 62, which is connected to a supply voltage, labeled 60.

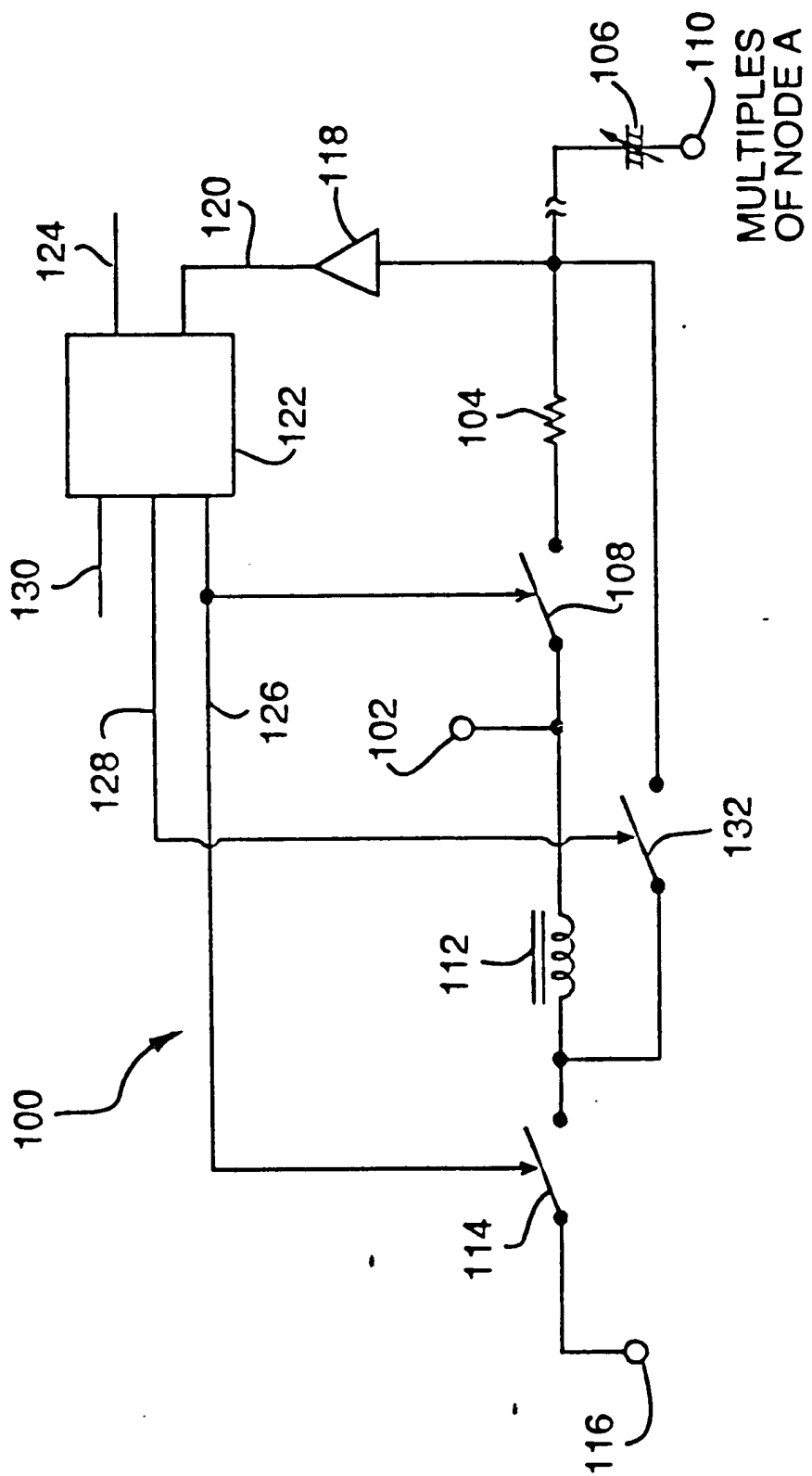


Fig. 4

08 447717

Fig. 5a

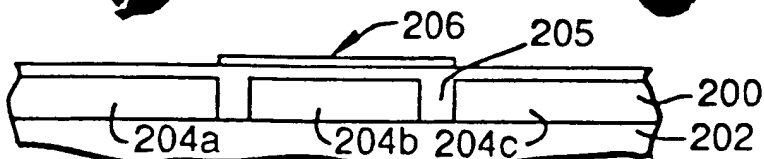


Fig. 5b

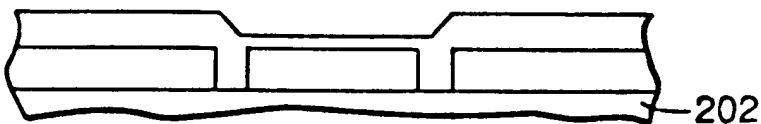


Fig. 5c



Fig. 5d

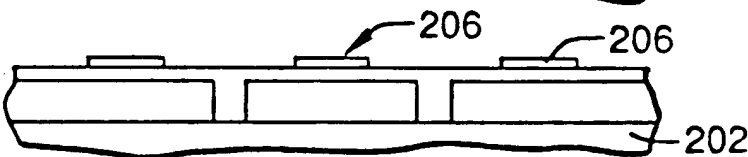


Fig. 5e

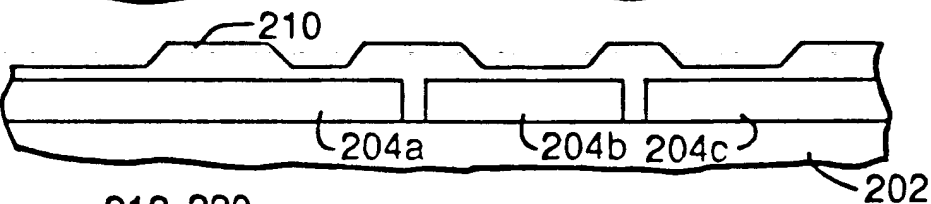


Fig. 5f

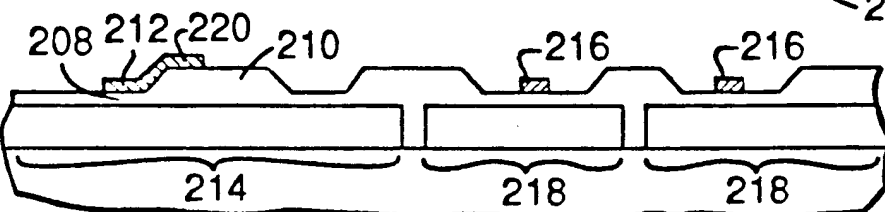


Fig. 5g

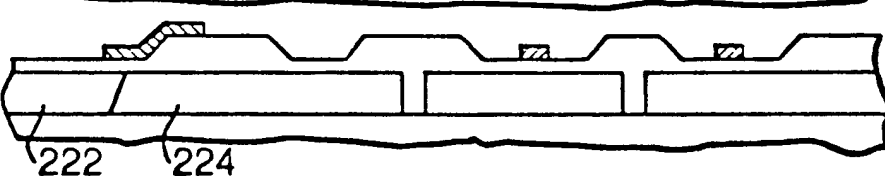


Fig. 5h

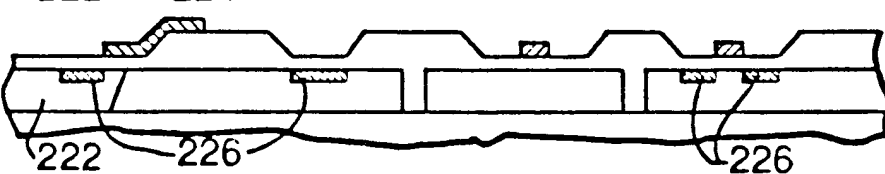


Fig. 5i

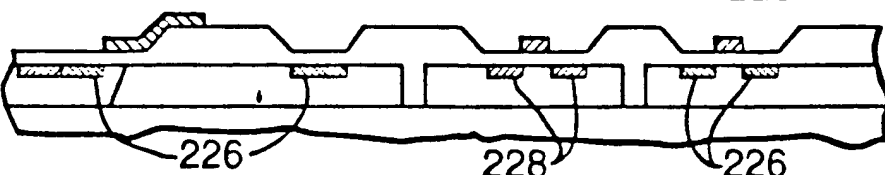
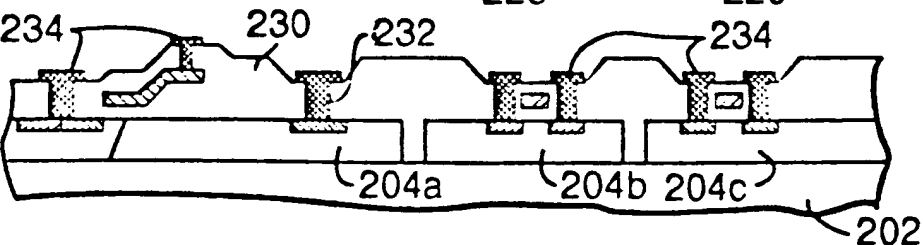


Fig. 5j



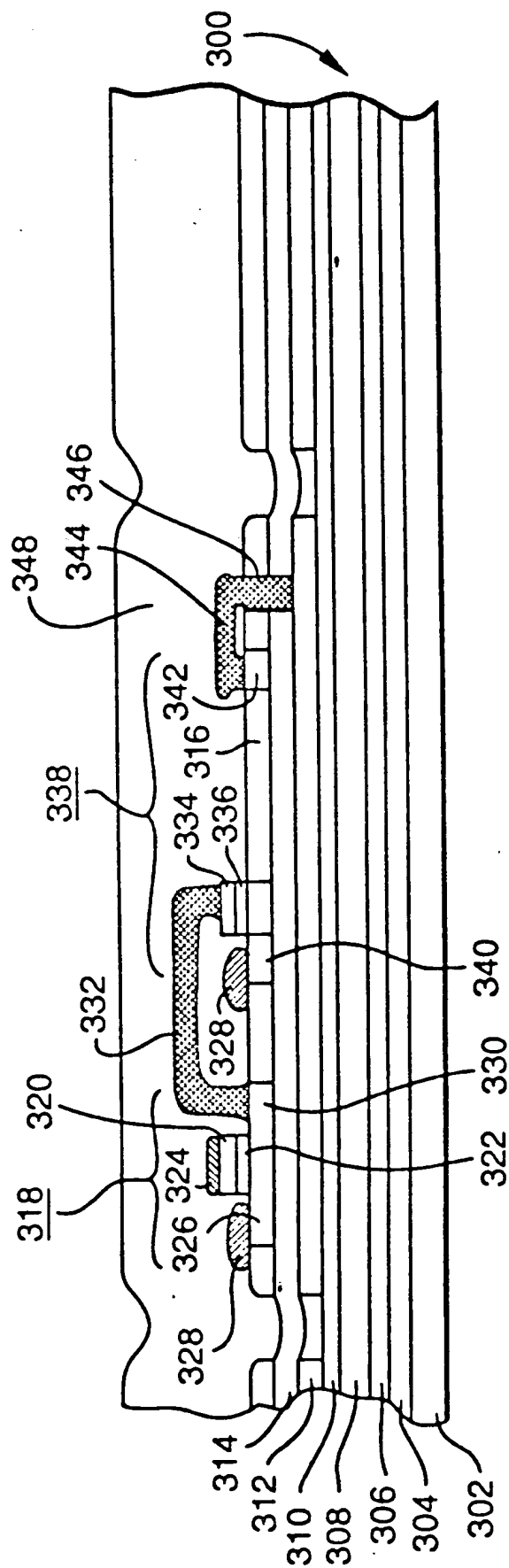


Fig. 6